

Solution note

“Back-end Semiconductor applications: Breaking through motion system solution to meet accuracy and throughput simultaneously”

Keywords:

Thermal decoupling, accuracy at tool point, C-shape, force path, metrology path, transient, reliability, absolute accuracy, throughput, cost of ownership, back-end solutions, Fan-Out Packages, FO-WLP, FO-PLP, flip chip die bonding, advanced packaging, μ -LED placement

Introduction

A tool selection in the semiconductor world is driven by Cost of Ownership (CoO). For back-end applications, CoO is typically defined as a combination of cost per bond and yield. Both are directly linked to positioning accuracy and throughput of the motion system.

By design, conventional motion system architectures are usually optimized either for high positioning accuracy or for high throughput.

Thanks to a very innovative motion system architecture, ETEL S.A. has released on the market a new platform able to meet simultaneously accuracy and throughput to an unprecedented level.

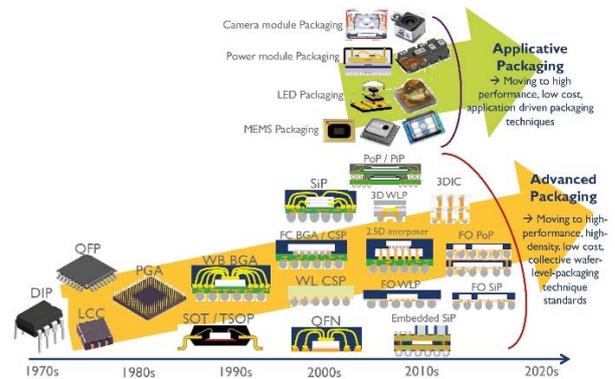
Under the name of TELICA, this new platform has been designed in the first place to fulfill the new and very stringent requirements of advanced packages such as FO-WLP (Fan-Out Wafer Level Package) and FO-PLP (Panel Level Fan-Out packages).

TELICA also covers perfectly the needs of all the flip-chip processes such as C4, C2, and Thermo Compressing Bonding (TCB).

As an example, a panel compatible TELICA platform used in FO-PLP offers a placement accuracy of one micrometer ($\pm 1 \mu\text{m}$), over a substrate size of 720x 650 mm, at a throughput higher than 3 kUPH.

Market drivers in advanced packaging

As shown in Fig.1, advanced packaging has gained quite a lot of complexity over the years.



Picture courtesy of Yole développement – www.yole.fr

Fig.1 Advanced packaging roadmap

The Ball Grid Array (BGA) packages evolved towards 2.5 and 3D packages, while the industry is now heading for Fan-Out packages. All those different types of packages are calling specific requirements from a placement perspective in terms of accuracy, throughput and force to be applied.

Flip-Chip processes

The most common packages produced through a flip-chip die bonding operation are calling for C4, C2 and TCB processes (Fig.2).

The **C4 process** is the historical die bonding process on chip with ball array with typical pitch of 120 μm . This process requires a placement accuracy of 10 μm at best since the chip is self-centering while going through the mass reflow process. Bonding force is limited to 50 N.

High throughput is required (around 15 kUPH).

The **C2 process** is calling for higher placement accuracy, the ball array being replaced by copper pillars. The pitch is finer (60 μm) and placement accuracy is in the range of 6 μm . Bonding force is limited to 50 N. High throughput is required (around 10+ kUPH).

The **TCB process** allows ultra fine pitch on the chip (<40 μm) while reflow is done locally through thermo-compression. The placement accuracy has to go down to 3 μm . Higher bonding force are needed, up to 250 N depending on the component. Throughput is limited by the process time, around 1.5 kUPH.

TCB process is driving the need of force to be applied in Z direction together with positioning accuracy.

The TCB process consisting in a local reflow of the C2 copper pillars with solder cap, throughput is a clear limiting factor for this process. It is therefore reserved for specific type of packages.

The advantages of TCB are for higher pin-count, finer pitch, thinner chips, higher-density, and thinner package substrates, and controlling warpage and die tilt.

C4, C2 and TCB are flip-chip processes calling for "short range accuracy".

This means that the accuracy is required over a very limited travel even if the working range can be quite large. This short range accuracy is driven by the distance between the up-looking camera and the bond head. Typically around 50 to 100 mm.

Fan-out packages

Although it was invented 20 years ago, Fan-Out package gained a lot of interest from the market as an alternative to the Fan-In mainly over the past five years.

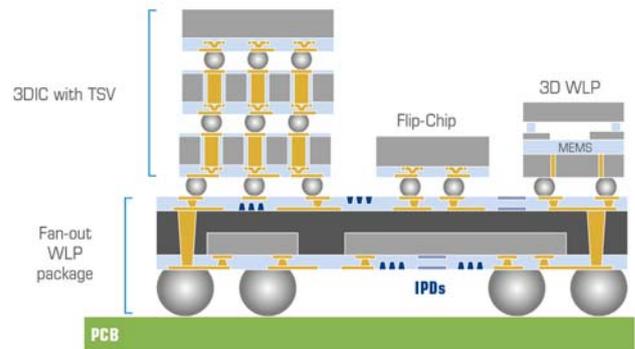


Fig.3 Lithography for advanced packaging

The dies becoming smaller and smaller, it gets difficult to ensure the electrical connection to the external world. With Fan-Out packages, the high density of interconnects of the small dies are redistributed through a specific ReDistribution Layer (RDL), allowing at the same time to embed other passive components in the overmolding (Fig.4).

The use of Fan-Out packages is driven by costs, form factor and density of interconnects.

C4 PROCESS	Normal pitch $\geq 120 \mu\text{m}$	 C4 FC (Controlled collapse chip connection)	Cold solder FC process <ul style="list-style-type: none"> flux dipping, mass reflow max. bond force 50 N accuracy 10 μm at 3 σ typical UPH 5'000 per head
C2 PROCESS	Fine pitch $\geq 60 \mu\text{m}$	 C2 FC (Chip connection)	Cold Cu-Pillar FC process <ul style="list-style-type: none"> flux dipping, mass reflow max. bond force 50 N accuracy 6 μm at 3 σ
THERMO COMPRESSION	Ultra fine pitch $\geq 40 \mu\text{m}$	 TC/LR FC (Thermocompression /Local reflow)	Hot Cu-Pillar FC process <ul style="list-style-type: none"> no flux, TC/LR (local reflow) up to 500 N bond force 3 μm at 3 σ (2 μm at 3 σ) typical UPH 1'200 per head

Fig.2 C4, C2 and TCB processes

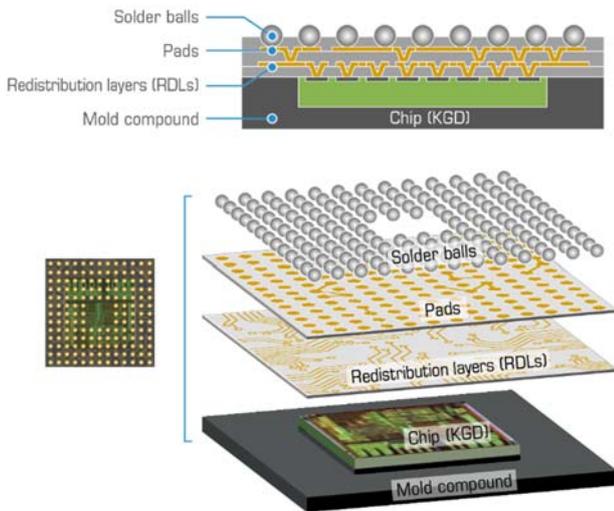
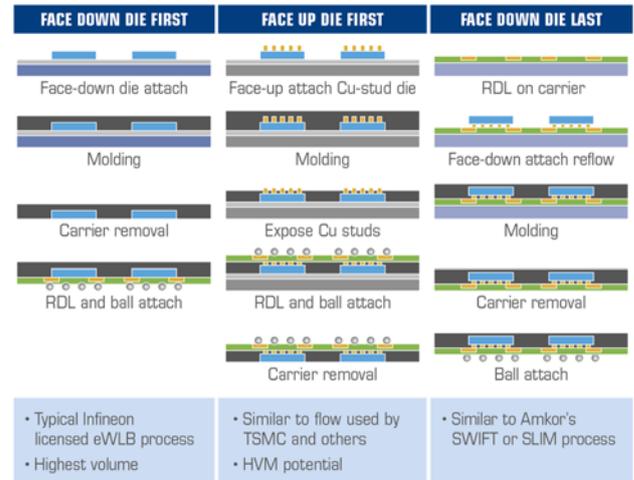


Fig.4 Fan-Out embedded wafer level packaging

Many Fan-Out options are under consideration from Die-first / RDL last, RDL first / Die last, face-up or face-down, all of the combinations benefiting from pros and cons.

While many challenges relate to the overall behavior of the different materials stack (carrier made of glass or steel, Die Attach Film, molding compound and so on), one of the first challenge relates to the die bonding process itself.

As shown in Fig.5, the placement accuracy is driven by the way the Fan-Out packages are built (die first or die last, face-up or face-down) and by the density of connections. The higher the density, the finer the connection pitch and the higher the placement accuracy requirements.



Accuracy and UPH are key metrics for equipment selection in all flows

Fig.5 Fan-out packages processes

The die bonding process dealing with Fan-out packages consist in picking Known Good Dies (KGD), usually from a source wafer and placing them on a temporary substrate, either a wafer or a panel. This populated substrate then goes through an over-molding process, and redistribution layers are deposited through a lithography process. The latter step is driving the need for placement accuracy at the bonding level.

The temporary substrate does not necessarily integrate any detectable marks allowing for a local alignment at landing of the bond head, as opposed to what is commonly used in Flip-chip processes (Fig.6). The motion system positioning the bond head in front of the substrate therefore needs to navigate over the full carrier with the proper global accuracy level ("long range" placement accuracy). When a fiducial is available for a local camera detection before landing, the placement accuracy is required over a limited travel also called "short range" placement accuracy.

Global placement accuracy can go down to the μm level over panels of more than 650 x 650 mm.

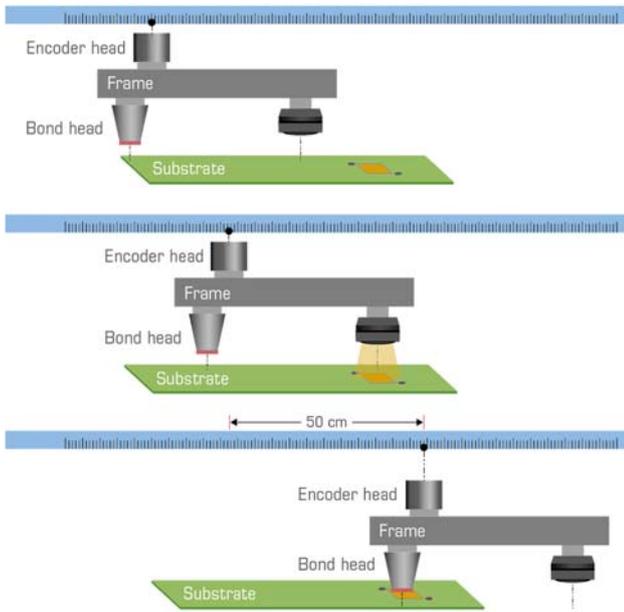
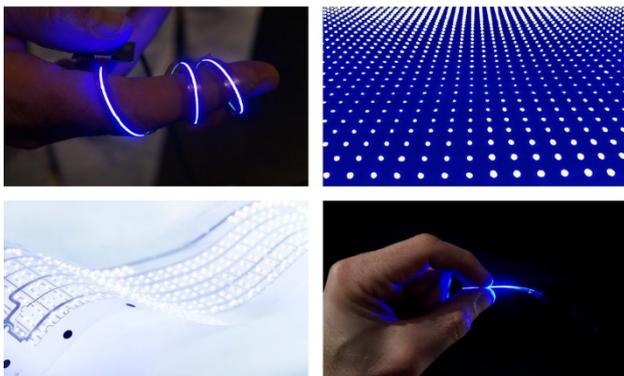


Fig.6 Die bonding process

μLED

μLED is an emerging technology targeting many commercial application from wearables, screens, heads-up monitoring (HUM), TV screens, and automotive to name a few.

The display business calling for low power consumption, high contrast, wide viewing angles, curved and flexible backplanes, Micro-LED can also bring many benefits on other devices such as odd shaped ones as shown in Fig.7.



Pictures courtesy of Rohinni - www.rohinni.com

Fig.7 LED applications

Micro-LEDs are much smaller and thinner than conventional LEDs (down to a couple of microns) and therefore pretty difficult to handle. They come in millions for each customer device and each micro LED needs to properly work and deliver the required performance level.

While many companies are working on mass transfer of those micro-LEDs to cope with very large screens, individual micro LED placement may be considered in some other applications (see Table 1).

DISPLAY TECHNOLOGY	LCD	OLED	MICRO LED
Mechanism	Backlight / LED	Self-emissive	Self-emissive
Contrast ratio	5'000:1	∞	∞
Lifespan	Medium	Medium	Long
Response time	ms	μs	ns
Operating temperature	-40 to 100°C	-30 to 85°C	-100 to 120°C
Power consumption	High	Medium	Low
View angle	Low	Medium	High
Pixel per inch	Up to 800 ppi	500 ppi	>2000 ppi
Cost	Low	Medium	High

Table 1 LED technology

Requirements in terms of placement accuracy can be in the range of $\pm 1.5 \mu\text{m}$ while a very high throughput is necessary.

Ultimately, the large TV screen application is a clear target for μLED which, on the motion system side, implies large travels, and super high throughput.

Fig.8 shows «the Wall» from Samsung, presented in January 2018 in CES show Las Vegas.



Fig.8 μ LED screen application

« The wall » is the largest TV screen ever made, with a 146" diagonal (365 cm) and 8.3 Millions of pixels displaying a full HD picture. Each pixel is a tryptic of 3 μ LED: Red (R), Green (G), Blue (B), which brings the Total amount of μ -LED to be placed at the level of 24.8 Millions!

Motion system architecture

The conventional C-shape model

From the very early ages of machine design, the cinematic architecture of a machine was based on the main concept that the part to be processed and the process tool itself are connected through a simple C-shaped arm.

This was already true in 1670 for one of the very first microscopes shown in Fig.9.

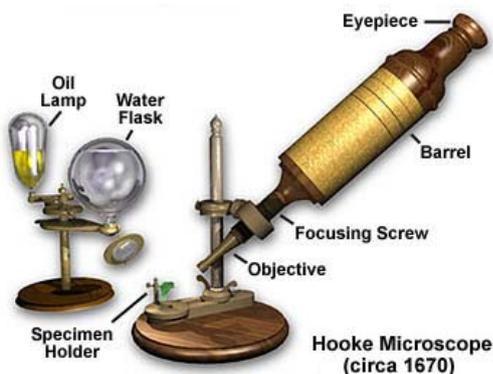


Fig.9 First microscope

The specimen holder and the optical device are connected together through a mechanical holder which can be depicted as a C-shape as can be seen in Fig.10.

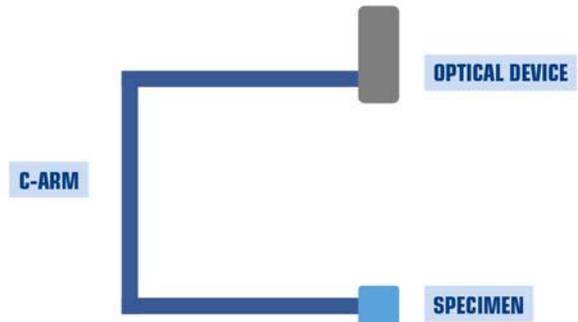


Fig.10 C-shape mechanical holder

The exact same concept is being applied to all conventional motion systems. Usually on the semiconductor front-end applications, the substrate (wafer) is to be moved in front of a fixed processing tool (ellipsometer for example). On the Semiconductor Back-end side, this is usually the opposite. The substrate (wafer, panel, die) remains static while the process tool (bond head for example) is moved above it. Whatever part is moved, both substrate and process tool are connected to each other through a C-arm (Fig. 11).

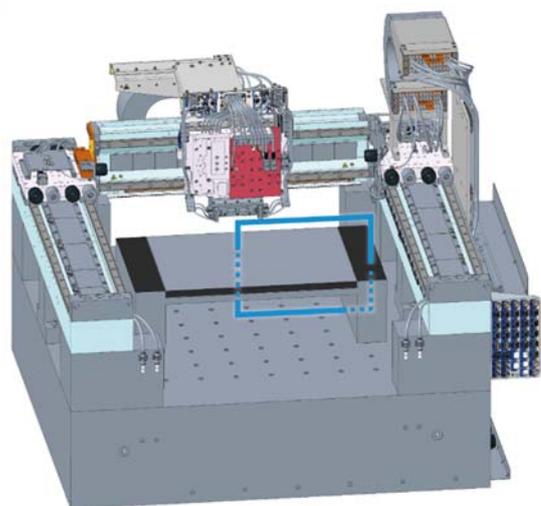


Fig.11 C-arm on a simple gantry system

The C-Shape implies that the metrology path to get the relative position between the substrate and the process is pretty long and thus subject to many environmental and mechanical distortions. Typically, an ambient temperature would lead to thermal expansion, thus affecting the relative positioning accuracy between the two elements.

In the case of a motion system, it is also clear that the forces generated by the motors moving the process tool and the metrology loop measuring the positioning of this head versus the substrate are on the same path. As a consequence, any vibration generated by the motor movement is therefore directly “detected” by the metrology piece of equipment, affecting the accuracy of the reading.

Moreover, the position encoders are located along the motors of each axis, which most of the time is quite far from the plane where the process is taking place. Abbe errors are thus becoming the main contributor to placement inaccuracy.

While breaking-through solutions such as maglev based solutions can be found to fully decouple both force and metrology paths, smart design around conventional C-shape solutions have demonstrated outstanding results.

This is what ETEL S.A. implemented by developing a new platform under the name of TELICA.

The non-conventional TELICA approach

Mechanical architecture

The mechanical architecture of the TELICA platform (see Fig.12) is not moving away from a C-Shape architecture. Yet, TELICA is introducing a very smart approach consisting in a secondary metrology loop, located at the process plane level - therefore heavily reducing the Abbe errors - and partially decoupled from the force path of the motors.

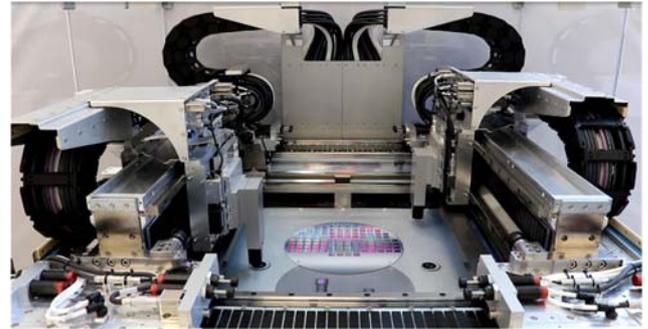


Fig.12 TELICA platform

This is a major improvement applied to a conventional dual gantry motion system moving in X, Y and Z directions.

The Moving Metrology Frame

The TELICA platform integrates as an option a Moving Metrology Frame (MMF). The MMF is composed of multi-dimensional encoders correcting the tool tip position in the X, Y and Rz Degrees of Freedom (Fig.13). It acts as a dual position feedback loop allowing the correction of the placement accuracy at the process plane level while running extremely high duty cycles and covering large working areas.

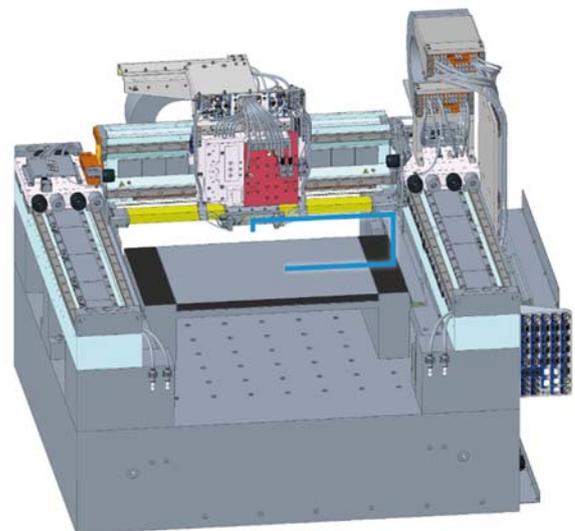


Fig.13 TELICA with moving metrology frame

The MMF is thermally-decoupled from the motion axes themselves, making it the holy reference along the bonding process.

A final $\pm 1 \mu\text{m}$ absolute positioning accuracy can be reached over the full panel size, at full dynamics, and whatever the working state of the machine (cold start, heating up, stabilized or cooling down), as shown on Fig.14.

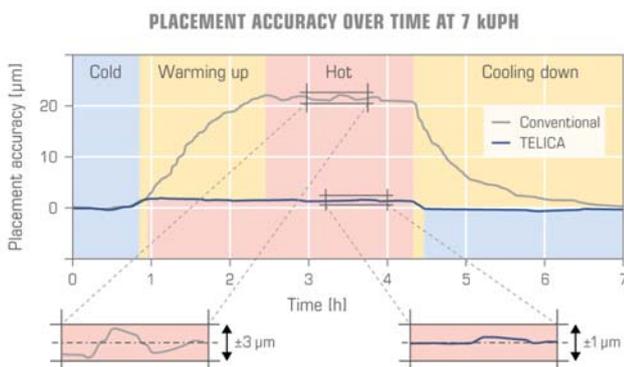


Fig.14 Placement accuracy of TELICA vs. conventional model

Water cooling as an answer to throughput demand

The powerful ironcore linear motors are water cooled to allow unprecedented, high accelerations (up to 80 m/s^2), and high duty cycles, while ensuring thermal stability, resulting in unprecedented placement accuracy.

State-of-the-art controllers

Coupled to the state-of-the-art Position and Motion controllers of ETEL S.A., the TELICA platform benefits from multiple control features such as:

Zero settling time, non-linear control, advanced feed-forward & trajectory filters, full synchronization of all axes with nanosecond jitter and specific gantry control algorithm, multidimensional mapping, advanced triggering capabilities based on real mapped position...

Advanced software diagnostic and system identification tools for control optimization.

TELICA platform

The TELICA platform is a motion system with a dual gantry architecture (Fig.15). It provides twice 3 Degrees of Freedom in X, Y and Z directions.



Fig.15 TELICA for panel level packages

TELICA has been developed under two standard variants, one dealing with wafer level packages (travels of around 420 mm in both X and Y directions), the second one coping with Panel level requirements (travels around 750 mm in both X and Y directions) (Fig.16).

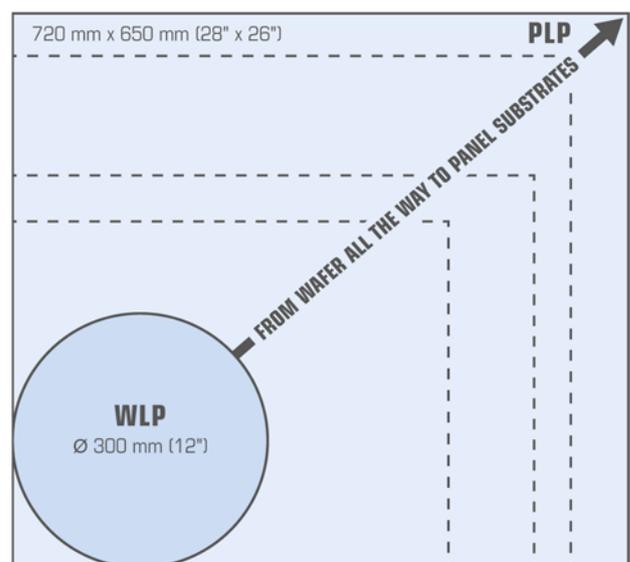


Fig.16 TELICA standard possibilities

Fig.17 shows a panel size application that is fully qualified as providing a $\pm 1 \mu\text{m}$ positioning accuracy at a throughput of 3.5 kUPH over a 720 x 650 mm panel.

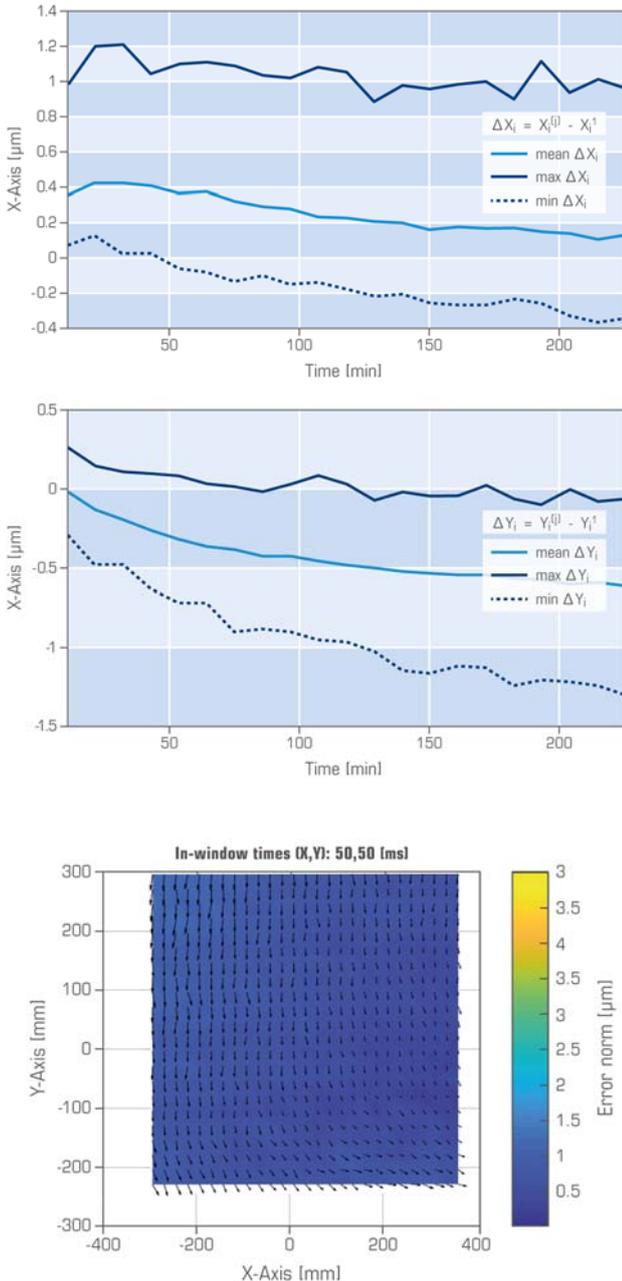


Fig.17 Position accuracy examples

Vibration isolation system

With a placement accuracy requirement hitting unprecedented levels on the back-end application side, vibrations coming from the floor and driving

forces generated by the motion of the system itself are definitely disturbances to take care about.



Fig.18 QuiET active isolation system

With its "Forward Integration Concept", ETEL S.A. is in a position to provide you with a turnkey solution integrating the vibration isolation part to the motion system. The ETEL's QuiET active isolation system (Fig.18) will bring machine to the next performance level in terms of move and settle, floor vibration immunity and process stability.

References

- [1] QuiET "The QuiET active isolation system" <https://www.etel.ch/motion-systems/active-isolation-system/>

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